What is claimed is:

1. An interfacing circuit comprising:

a command decoder which decodes an input packet command and generates first through N-th commands;

an operation controller which generates first through N-th operation signals for performing operations corresponding to the commands in response to a clock signal; and

a transmission controller which transmits the first through N-th operation signals as first through N-th control signals in response to the clock signal,

wherein the transmission controller comprises a reset signal generator which generates a reset signal for interrupting the transmission of the first control signal, when multiple commands of the first through N-th commands are generated simultaneously.

2. The interfacing circuit of claim 1, wherein the operation controller comprises first through N-th operation units which receive the first through N-th commands output from the command decoder and generate the first through N-th operation signals.

3. The interfacing circuit of claim 2, wherein each of the first through N-th operation units comprises:

a master signal generator which receives and outputs a corresponding command as a master signal in response to the clock signal; and

a combinational logic unit which generates a corresponding operation signal in response to the master signal,

wherein the first operation unit includes a first master signal generator which receives and outputs a corresponding command as a first master signal in response to the clock signal.

4. The interfacing circuit of claim 3, wherein the reset signal generator comprises:

a first switching unit which connects a source voltage to a first node in response to an inverted signal of the first master signal;

a second switching unit which connects a ground voltage to a second node in response to the first master signal;

a third switching unit which connects the first node to the second node when any of the master signals other than the first master signal is activated; and

a reset controller which generates the reset signal when any of the master signals other than the first master signal is activated simultaneously with the first master signal, in response to a signal at the first node, the inverted signal of the first master signal, and a reset control signal.

5. The interfacing circuit of claim 4, wherein the first switching unit is a PMOS transistor having a gate to which the inverted signal of the first master signal is applied, and the second switching unit is an NMOS transistor having a gate to which the first master signal is applied.

6. The interfacing circuit of claim 4, wherein the third switching unit is comprised of a plurality of NMOS transistors, each having a gate to which the master signals other than the first master signal are applied respectively, and which are connected in parallel between the first node and the second node.

7. The interfacing circuit of claim 4, wherein the reset controller comprises:

a NOR means which performs a NOR operation on a signal at the first node and an inverted signal of the first master signal to be output as the reset signal;

a first inverter between an output node of the NOR means and the first node which inverts the reset signal to apply to the first node; and

an NMOS transistor which connects the output node of the NOR means to a ground voltage in response to the reset control signal.

8. The interfacing circuit of claim 3, wherein the first master signal, the first operation signal, and the first control signal are the same signal for activating a sensing operation of a memory core.

9. The interfacing circuit of claim 1, further comprising a memory core of a semiconductor memory receiving the first through N-th control signals.

10. The interfacing circuit of claim 1, wherein the transmission controller comprises first through N-th flip-flops which output the first through N-th operation signals as the first through N-th control signals, respectively, in response to the clock signal.

11. The interfacing circuit of claim 1 installed in a Rambus DRAM.

12. The interfacing circuit of claim 1 wherein the commands incorrectly operate a circuit receiving the first through N-th control signals when the multiple commands are generated simultaneously, if the transmission of the first control signal was activated.

13. The interfacing circuit of claim 1 wherein the first control signal activates a sensing operation of a memory core.